Reverse Templating Effects of Low-Resistivity Ru ALD on Sputtered Ru

Victor Wang Materials Science and Engineering Materials Science and Engineering UC San Diego La Jolla, USA viw031@eng.ucsd.edu

Chenghsuan Kuo UC San Diego La Jolla, USA c2kuo@eng.ucsd.edu

Ravindra Kaniolia **EMD** Electronics Haverhill, USA ravindra.kanjolia@emdgroup.com mansour.moinpour@emdgroup.com

Mansour Moinpour **EMD Electronics** San Jose, USA

Jacob Woodruff **EMD** Electronics Haverhill, USA jacob.woodruff@emdgroup.com

Harsono Simka Samsung Electronics San Francisco, USA h.simka@samsung.com

Andrew C. Kummel Chemistry and Biochemistry UC San Diego La Jolla, USA akummel@ucsd.edu

Abstract— Ruthenium is a promising candidate to replace Cu as an interconnect metal due to its low resistivity in narrow vias and resistance to electromigration. In previous work, a Ru Atomic Layer Deposition (ALD) process using Ru(CpEt)2 and O2 was developed to produce films with bulk-like resistivities. However, the ALD exhibits poor initial nucleation with variable initial nucleation delay causing thickness control to be difficult and high surface roughness. In this work, the effects of depositing low resistivity ALD Ru on 2 and 10-nm sputtered Ru films are investigated to eliminate the initial poor nucleation while retaining low overall film resistivity.

Keywords—atomic layer deposition, ruthenium, interconnect metallization

I. BACKGROUND AND EXPERIMENT

Cu has been used as the interconnect metal of choice since the early 2000s [1]. However, as modern CMOS nodes continue to decrease pitch lengths and via widths, the effective resistivity of Cu in the M0/M1 interconnect layers increases, motivating the use of alternate metals such as Co or Ru. Ru is of special interest owing to its short electron mean-free-path allowing for lower effective resistivity in narrow (<10nm) via widths compared to Co or Cu [2][3]. While many Ru ALD processes are available, the search for a low-resistivity Ru process is ongoing. One previously reported process using the Ru(CpEt)2 precursor and O₂/He as a co-reactant yielded films with bulklike resistivity [4]. However variable initial nucleation delay causes difficulties in controlling thicknesses for thin films below 15 nm and results in high surface roughness in thicker films. By growing ALD Ru on sputtered Ru, the initial nucleation delay can be eliminated. At high temperatures throughout the lengthy ALD deposition process, the grain structure of the underlying sputtered seed layer may be reverse-templated by the growth of ALD film, which could result in a resistivity lower than that of sputtered films.

In this report, Ru ALD was performed on sputtered Ru seed layers using the Ru(CpEt)₂ (EMD Electronics) with O₂ as a coreactant. The ALD process was performed at 360 °C deposition temperature at a pressure of ~1 Torr. The sputtered 2 and 10 nm Ru seed layer was deposited with the Denton Discovery 635 using 100 W sputter power at a 3mTorr pressure for 17 s at a substrate temperature close to 25 °C. Combinations of both processes were performed on SiO₂, and sapphire samples. Prior to deposition, samples were degreased with acetone, methanol, and DI water, followed by 30 minute ultra-high-vacuum anneal at 350 °C to remove atmospheric contaminants. After deposition, select samples were transferred under vacuum to the attached UHV chamber for XPS (Scienta Omicron). Due to the overlap in binding energy between the C1s and Ru 3d XPS peaks, precise deconvolution of the two peaks is not possible and a rough quantitative estimate is given for the C content. 4-pointprobe (Ossila Four-point-probe System, Ossila, Ltd.) measurements were performed after deposition was completed on films of dimensions 6 mm x 2 mm for SiO_2 and 6mm x 3mm for sapphire using a probe spacing of 1.27mm. XRR measurements were performed on the films to determine film thicknesses.

II. SUB-10NM FILM WITH $Ru(CPET)_2 + O_2$ on sputtered RU

A study was performed using the cyclopentadienyl-based Ru precursor, Ru(CpEt)₂ with O₂ as a co-reactant. The ALD was performed on both bare SiO₂ and on SiO₂ with 2 nm of sputtered Ru. Fig. 1 shows XPS quantification for Ru ALD at 360°C on both samples after 70 cycles of deposition. On bare SiO₂, XPS still yields strong substrate signal, which implies that deposition is still no thicker than 4 nm. Conversely, on the 2 nm sputtered Ru sample substrate signal is no longer seen. Furthermore, XRR fringes with their respective fit shown in Fig. 2 yield a thickness estimate of about 8.34nm. Subtracting the 2 nm of sputtered Ru deposition, ~6 nm of Ru was deposited via ALD on the sputtered Ru sample. The contrast in growth rate between both samples is consistent with poor initial nucleation of the ALD process on bare SiO₂. Ex-situ Four-point probe measurement also resulted in a measured sheet resistance of 10 Ω/\Box , which translates to 8.34 $\mu\Omega$ cm when taking into account the film thickness This resistivity is below that of sputtered Ru in literature, especially at such a low film thickness. The low resistivity value measured is consistent with the Ru ALD's ability to reverse-template the underlying sputtered Ru layer resulting in large grain sizes favorable for lower resistivity values.



Fig. 1. XPS of Ru ALD at 360 °C with $Ru(CpEt)_2 + O_2$ on (a) bare SiO₂ substrate exhibiting high substrate signal implying little deposition (b) 2nm of sputtered Ru on SiO₂ showing a completely buried sample with no SiO₂ substrate signal. Additionally low O1s signal indicates Ru film without much oxygen contamination.



Fig. 2. XRR of 70 cycles of Ru ALD at 360 °C with $Ru(CpEt)_2 + O_2$ on 2 nm of sputtered Ru on SiO₂ showing good fit of the modeled curve to the measured curve giving confidence in the 8.34nm thickness value attained.

III. SNEAK CURRENT VERIFICATION ON SAPPHIRE

The low resistivity measured could be artificial due to sneak current conducting through the sample edges to the semiconducting back side of the substrate. To verify that this is not the case, a similar study was done on insulating sapphire substrates. 2 nm of sputtered Ru was deposited first as a seed layer then followed by 350 cycles of the Ru ALD. Additionally, a forming gas anneal at 450°C for 30 minutes was performed. Four-point probe measurement resulted in a measured sheet resistance of 3.76 Ω/\Box . Fig. 3 shows the XRR fringe patterns along with the modeled curve, which yielded a film thickness of 21.5nm. This translates to a film resistivity of 8.09 $\mu\Omega$ cm. With the low resistivity still present for an insulating substrate, the possibility of sneak current producing artificially low resistivity values was eliminated.



Fig. 3. XRR of 350 cycles of Ru ALD at 360 °C with $Ru(CpEt)_2 + O_2$ on 2nm of sputtered Ru on sapphire showing good fit of the modeled curve to the measured curve giving confidence in the 21.5nm thickness value attained.

IV. REVERSE-TEMPLATING OF 10 NM SPUTTERED RU

While the ALD Ru process seemed to reverse-template the sputtered film in Fig. 1 and Fig. 2, the effect could be possible only due to the sputtered seed layer being thin. A second study was done with a thicker sputtered seed layer of 10 nm instead to verify the reverse templating effect on a thicker Ru film. 300 cyles of Ru ALD were performed on a sample with 10 nm of sputtered Ru on SiO₂. Four-point probe measurement resulted in a measured sheet resistance of 2.51 Ω/\Box . Fig. 4 shows the XRR fringe patterns and fit, which yielded a thickness of 34.8 nm, which results in an overall resistivity of 8.73 $\mu\Omega \cdot cm$. The low resistivity value despite the thicker 10 nm sputtered Ru seed layer is consistent with the ALD process reverse-templating the underlying sputtered Ru resulting in a grain structure that is more favorable towards lower resistivity.



Fig. 4. XRR of 300 cycles of Ru ALD at 360° C with Ru(CpEt)₂ + O₂ on 10nm sputtered Ru on SiO₂. Fit to the measured curve's frequency matches well enough to give confidence in the thickness value of 31.5nm.

Fig. 5 shows a TEM image of the deposited film. From the TEM image, the overall film thickness can be estimated to roughly 39nm, which is fairly close to the estimated thickness from XRR. There is some degree of non-uniformity seen in the TEM image that can be attributed to unideal conditions in the

sputtering process. Large grains are visible from the TEM image confirming the reverse templating effect of the ALD process on the 10nm sputtered Ru seed layer. Additionally, no seam is seen between the ALD layer and the sputtered layer, which is also consistent with the reverse templating effect discussed.



Fig. 5. TEM image of 300 cycles of Ru ALD at 360° C with Ru(CpEt)₂ + O₂ on 10nm sputtered Ru on SiO₂. Large clear grains can be observed in the image while no seam is visible between the sputtered and ALD layers.



Fig. 6. Resistivity-thickness plot comparing DC sputtered films from literature and this work's reverse templated films.

Reverse-templating effect of ALD Ru on an underlying sputtering layer is demonstrated in this work. The shown data is consistent with the high temperature Ru ALD process altering the grain structure of the underlying sputtered film for larger grain sizes, enabling competitively low resistivity values between 8-9 $\mu\Omega$ cm. Fig. 6 shows a resistivity vs thickness benchmarking plot comparing our reverse templated films to DC sputtered films from Dutta et al. [6]. This reverse-templating effect is consistently seen even when changing the underlying sputtered Ru layer thickness from 2nm to 10nm. By taking advantage of this reverse templating effect, thick layers of low resistivity blanket Ru can be deposited quickly for applications in semi-damascene schemes when compared to depositing only with ALD. However, further work remains to investigate the limits of this reverse-templating effect with regard to the seed layer thickness and ALD layer thickness.

ACKNOWLEDGMENT

This work is supported by the Center for Heterogeneous Integration of Micro Electronic Systems (CHIMES), a Semiconductor Research Corporation program sponsored by JUMP and DARPA.

REFERENCES

- L. Chen, N. Magtoto, B. Ekstrom, J. Kelber, "Effect of surface impurities on the Cu/Ta interface," *Thin Solid Films* 376, 115-123 2000.
- [2] D. Gall, "The search for the most conductive metal for narrow interconnect lines," J. Appl. Phys. 127, 050901 2020.
- [3] M. H. van der Veen, N. Heylen, O. Varela Pedreira, I. Ciofi, S. Decoster, V. Vega Gonzalez, N. Jourdan, H. Struyf, K. Croes, C. J. Wilson, Zs. Tokei, "Damascene benchmark of Ru, Co and Cu in scaled dimensions," *Proc. of the IITC 2018*, 172 2018.
- [4] M. Breeden, V. Wang, R. Kanjolia, M. Moinpour, J. Woodruff, H. Simka, A. Kummel, "Low Resistivity Ru ALD for Interconnects," *IITC, 2022.*
- [5] L. Vitos, A. V. Ruban, H. L. Skriver, J. Kollar, "The surface energy of metals," Surf. Sci. 411, 186-202 1998.
- [6] S. Dutta, K. Sankaran, K. Moors, G. Pourtois, S. V. Elshocht, J. Bommels, W. Vandervorst, Z. Tokei, C. Adelmann, "Thickness dependence of the resistivity of platinum-group metal thin films," *J. Appl. Phys.* 122, 025107 2017.